WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first field effect transistor including a source and a gate and disposed in a silicon carbide substrate; and

a second field effect transistor including a drain and a gate and disposed in the substrate,

wherein the drain of the second field effect transistor connects to the source of the first field effect transistor, and

wherein the gate of the second field effect transistor connects to the gate of the first field effect transistor.

2. The device according to claim 1, further comprising:

a metal-oxide semiconductor field-effect transistor including a drain and a source and disposed in a silicon substrate,

wherein the second field effect transistor further includes a source,

wherein the drain of the metal-oxide semiconductor field-effect transistor connects to the source of the second field effect transistor, and

wherein the source of the metal-oxide semiconductor field-effect transistor connects to the gate of the second field effect transistor.

3. The device according to claim 2,

wherein the metal-oxide semiconductor field-effect transistor becomes an on-state in a case where the gate of the metal-oxide semiconductor field-effect transistor is applied with

a gate voltage in a range between 5 volts and 10 volts.

4. A semiconductor device comprising:

a first field effect transistor having a source and a gate and disposed in a silicon carbide substrate; and

a second field effect transistor having a drain and a source and disposed in the substrate,

wherein the drain of the second field effect transistor connects to the source of the first field effect transistor, and

wherein the source of the second field effect transistor connects to the gate of the first field effect transistor.

5. The device according to claim 1,

wherein the substrate includes:

a first layer made of silicon carbide and heavily doped with a first impurity having a first type conductivity;

a second layer made of silicon carbide and lightly doped with the first impurity; and

a third layer made of silicon carbide and moderately doped with the first impurity,

wherein the second layer is disposed on the first layer, and the third layer is disposed on the second layer,

wherein the substrate further includes:

a first impurity diffusion region heavily doped with the first impurity; and

a second impurity diffusion region heavily doped with a second impurity having a second type conductivity,

wherein the second impurity diffusion region is disposed in the second layer near a boundary between the second layer and the third layer, and covers a predetermined area of the boundary,

wherein the third layer has first, second and third surface portions, and the first impurity diffusion region is disposed in each of the first, second and third surface portions of the third layer,

wherein the first field effect transistor is a vertical type junction field effect transistor having the source, the gate, a drain and a channel,

wherein the source of the first field effect transistor is the first impurity diffusion region disposed in the first surface portion, the drain of the first field effect transistor is the first layer, the gate of the first field effect transistor is the second impurity diffusion region, and the channel of the first field effect transistor is a part of the second layer near the boundary between the second layer and the third layer, the part of the second layer not being covered with the second type impurity diffusion region,

wherein the second field effect transistor is a lateral type junction field effect transistor having a source, the gate, the drain and a channel,

wherein the source of the second field effect transistor is the first impurity diffusion region disposed in the second surface portion, the drain of the second field effect transistor is the first impurity diffusion region disposed in the third surface portion, the gate of the second field effect transistor is the second impurity diffusion region, and the channel of the second field effect

transistor is the third layer, and

wherein the second surface portion separates from the third surface portion.

6. The device according to claim 4,

wherein the substrate includes:

a first layer made of silicon carbide and heavily doped with a first impurity having a first type conductivity;

a second layer made of silicon carbide and lightly doped with the first impurity; and

a third layer made of silicon carbide and moderately doped with the first impurity,

wherein the second layer is disposed on the first layer, and the third layer is disposed on the second layer,

wherein the substrate further includes:

a first impurity diffusion region heavily doped with the first impurity; and

a second impurity diffusion region heavily doped with a second impurity having a second type conductivity,

wherein the second impurity diffusion region is disposed in the second layer near a boundary between the second layer and the third layer, and covers a predetermined area of the boundary,

wherein the third layer has first, second and third surface portions, and the first impurity diffusion region is disposed in each of the first, second and third surface portions of the third layer,

wherein the first field effect transistor is a vertical type

junction field effect transistor having the source, the gate, a drain and a channel,

wherein the source of the first field effect transistor is the first impurity diffusion region disposed in the first surface portion, the drain of the first field effect transistor is the first layer, the gate of the first field effect transistor is the second impurity diffusion region, and the channel of the first field effect transistor is a part of the second layer near the boundary between the second layer and the third layer, the part of the second layer not being covered with the second type impurity diffusion region,

wherein the second field effect transistor is a lateral type accumulation mode field effect transistor having the source, a gate, the drain and a channel,

wherein the source of the second field effect transistor is the first impurity diffusion region disposed in the second surface portion, the drain of the second field effect transistor is the first impurity diffusion region disposed in the third surface portion, the gate of the second field effect transistor is provided by an electrode disposed on the third layer through an insulation film and disposed between the second and third surface portions, and the channel of the second field effect transistor is the third layer, and

wherein the second surface portion separates from the third surface portion.

7. The device according to claim 4,

wherein the substrate includes:

a first layer made of silicon carbide and heavily doped with a first impurity having a first type conductivity;

a second layer made of silicon carbide and lightly doped with the first impurity; and

a third layer made of silicon carbide and moderately doped with the first impurity,

wherein the second layer is disposed on the first layer, and the third layer is disposed on the second layer,

wherein the substrate further includes:

a first impurity diffusion region heavily doped with the first impurity having the first type conductivity;

a second impurity diffusion region heavily doped with a second impurity having a second type conductivity; and

a third impurity diffusion region moderately doped with the second impurity,

wherein the second impurity diffusion region is disposed in the second layer near a boundary between the second layer and the third layer, and covers a predetermined area of the boundary,

wherein the third layer has first, second and third surface portions, and the third impurity diffusion region is disposed in a fourth surface portion of the third layer,

wherein the first impurity diffusion region is disposed in each of the first, second and third surface portions of the third layer,

wherein the first field effect transistor is a vertical type junction field effect transistor having the source, the gate, a drain and a channel,

wherein the source of the first field effect transistor is the first impurity diffusion region disposed in the first surface portion, the drain of the first field effect transistor is the first layer, the gate of the first field effect transistor is the second impurity diffusion region, and the channel of the first field effect transistor is a part of the second layer near the boundary between the second layer and the third layer, the part of the second layer without covering with the second impurity diffusion region,

wherein the second field effect transistor is a lateral type inverse mode field effect transistor having the source, a gate, the drain and a channel,

wherein the source of the second field effect transistor is the first impurity diffusion region disposed in the second surface portion, the drain of the second field effect transistor is the first impurity diffusion region disposed in the third surface portion, the gate of the second field effect transistor is provided by an electrode disposed on the third impurity diffusion region through an insulation film and disposed between the second and third surface portions, and the channel of the second field effect transistor is the third impurity diffusion region, and

wherein the second surface portion separates from the third surface portion, and the second and third surface portions contact the third impurity diffusion region.

8. The device according to claim 5, further comprising:

a separation disposed in the third layer and reaches the second impurity diffusion region,

wherein the separation separates the third layer into a first part and a second part, and

wherein the source of the first field effect transistor is disposed in the first part, and the second field effect transistor is disposed in the second part.

9. The device according to claim 8,

wherein the second impurity diffusion region covers almost whole area of the boundary between the second layer and the third layer except for the channel of the first field effect transistor, and

wherein the second impurity diffusion region separates between the second part and the second layer.

10. A method for manufacturing a semiconductor device including a lateral type field effect transistor and a vertical type junction field effect transistor, which are integrated in a silicon carbide substrate, the method comprising the steps of:

preparing a first layer made of silicon carbide and heavily doped with a first impurity having a first type conductivity, the first layer being to be a drain of the junction field effect transistor;

forming a second layer on the first layer, the second layer being made of silicon carbide and lightly doped with the first impurity and to be a channel of the junction field effect transistor;

forming a second impurity diffusion region heavily doped with a second impurity having a second type conductivity, disposed in

a predetermined surface portion of the second layer, and being to be a gate of the junction field effect transistor;

forming a third layer made of silicon carbide, moderately doped with the first impurity, and disposed on both of the second layer and the second impurity diffusion region; and

forming a first impurity diffusion region heavily doped with the first impurity, disposed in each of first, second third surface portions of the third layer, and being to be a source of the junction field effect transistor and a source and drain of the lateral type field effect transistor, respectively.

11. The method according to claim 10, further comprising the step of:

forming a separation disposed in the third layer to reach the second impurity diffusion region,

wherein the separation separates the third layer into a first part and a second part, and

wherein the source of the junction field effect transistor is disposed in the first part, and the lateral type field effect transistor is disposed in the second part.

12. The method according to claim 11,

wherein the step of forming the separation includes the steps of:

forming a trench in the third layer to reach the second impurity diffusion region; and

forming an insulation film on a sidewall of the trench.

13. The method according to claim 10,

wherein the second impurity diffusion region covers almost whole area of the predetermined surface portion of the second layer except for the channel of the first field effect transistor.

14. The method according to claim 10,

wherein the lateral type field effect transistor is a lateral type junction field effect transistor having a gate and a channel, and

wherein the gate of the lateral field effect transistor is the second impurity diffusion region, and the channel of the lateral field effect transistor is the third layer.

15. The method according to claim 14,

wherein the drain of the lateral type field effect transistor connects to the source of the junction field effect transistor, and

wherein the gate of the lateral type field effect transistor connects to the gate of the junction field effect transistor.

16. The method according to claim 10,

wherein the lateral type field effect transistor is a lateral type accumulation mode field effect transistor having a gate and a channel, and

wherein the gate of the lateral field effect transistor is provided by an electrode disposed on the third layer through an insulation film and disposed between the source and drain of the lateral type field effect transistor, and the channel of the lateral

type field effect transistor is the third layer.

17. The method according to claim 16,

wherein the drain of the lateral type field effect transistor connects to the source of the junction field effect transistor, and

wherein the source of the lateral type field effect transistor connects to the gate of the junction field effect transistor.

18. The method according to claim 10, further comprising the step of:

forming a third impurity diffusion region moderately doped with the second impurity, and disposed in a fourth surface portion of the third layer,

wherein the lateral type field effect transistor is a lateral type inverse mode field effect transistor having a gate and a channel, and

wherein the gate of the lateral field effect transistor is provided by an electrode disposed on the third impurity diffusion region through an insulation film and disposed between the source and drain of the lateral type field effect transistor, and the channel of the lateral type field effect transistor is the third impurity diffusion region.

19. The method according to claim 18,

wherein the drain of the lateral type field effect transistor connects to the source of the junction field effect transistor, and

wherein the source of the lateral type field effect transistor

connects to the gate of the junction field effect transistor.